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EXAMINER	
PAPPAS, PETER	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,953	SEILER ET AL.	
	Examiner	Art Unit	
	PETER-ANTHONY PAPPAS	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-15,19 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-15,19 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 14, 15, 25, 28 and 29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 101 set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-11, 13-15, 19 and 23-30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Said claims fail to fall within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing (May 15, 2008 memorandum issued by Deputy Commissioner for Patent Examining Policy, John J. Love, titled "Clarification of 'Processes' under 35 U.S.C. 101"). The instant claims neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-11, 13, 19, 23, 24, 26, 27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aila et al. (U.S. Pub. No. US 2005/0134588 A1) in view of Greene et al. (U.S. Patent No. 5, 579, 455).

6. In regard to claim 1 Aila et al. teach comparing a tile Z value range ("...In the following embodiments, the Z-fail version of the shadow volume algorithms is used as an example ... the Z-pass version is equally applicable..." – p. 3, ¶ 49; "...the following extra information is often stored for each tile: the minimum of all depth values in the tile, z_{min}, and the maximum of all depth values in the tile, z_{max}. It is appreciated that for processing shadow information more efficiently, a new concept may be introduced. The perimeter of the tile and the minimum and maximum depth values define a tile volume. For a rectangular tile, for example, the tile volume is a three-dimensional axis-aligned box in screen space, defined by the horizontal and vertical bounds of the rectangular tile together with the z_{min} and z_{max} values." – p. 4, ¶ 53) of a tile ("When images are processed, the frame buffer ... containing pixels of an image is typically divided into sets of pixels often called tiles ... The size of the tiles may vary..." – pp. 3, 4, ¶ 52) with a stencil code (e.g., shadow information, wherein said shadow information is processed after the execution of said Z-fail algorithm; Fig. 4, elements 404, 407 and 411; "When the shadow polygons are processed using the Z-fail algorithm, it is appreciated that those parts of the shadow polygons that are completely in front of previously rendered geometry, cannot affect the shadow mask. It is therefore noted that there is no need to

process these parts of the shadow polygons in the Z-fail algorithm. Two different categories of shadow polygons remain: shadow polygons that are completely hidden behind the previously rendered geometry and shadow polygons that intersect with the tile volume of a tile." – p. 4, ¶ 56).

It is noted that Aila et al. fail to teach a minimum pixel count for a tile and thus it is noted that a given tile is considered to read on either a single or a plurality of pixels. It is further noted that the respective claim language fails to disclose what exactly constitutes a "stencil code" and thus a stencil code is considered to read on shadow information.

However, Aila et al. fails to teach wherein said comparing comprises comparing a tile Z value range of a tile with a hierarchical Z value range. Greene et al. teach comparing a Z value range of a tile with a hierarchical Z value range (Abstract; "...the technique augments traditional Z-buffer scan conversion with an image-space Z-pyramid that allows the algorithm to reject hidden geometry very quickly..." – col. 3, ll. 56-64; "...When the basic test fails to show that a polygon is hidden, we go to the next finer level in the pyramid where the previous pyramid region has been divided into four quadrants. Here we attempt to prove that the polygon is hidden in each of the quadrants it intersects. For each of these quadrants, we compare the nearest Z value of the primitive to the value in the Z-pyramid. If the Z-pyramid value is closer, we know the primitive is hidden in the quadrant. If we fail to prove that the primitive is hidden in one of the quadrants, we go to the next finer level of the pyramid for that quadrant and try again. Ultimately, we either prove that the entire polygon is hidden, or we recurse down

to the finest level of the pyramid … This recursire test culls a substantial fraction of the hidden primitives in an efficient manner." – col. 6, ll. 9-36; col. 10, ll. 8-67; col. 11, ll. 1-3; "…it will be seen that it may be desirable to include not only Z-max elements in a depth buffer such as 502, but also Z-min elements. That is, each of the depth elements 512 can contain not only a Z-max element having the farthest depth of any display cell covered by the depth element 512, but also a Z-min element containing the nearest depth value of any of the display cells 204 covered by the depth element 512." – col. 11, ll. 4-12; "The Build Depth Buffer step 719 ... Within each level, an inner iteration is performed to visit each of the depth elements (Z-max elements) in that level. For each such Z-max element, the depth value which is written into that element is the farthest depth value in any of the Z-max elements which are covered by such Z-max element in the next finer granularity level. If the depth buffer 502 also includes Z-min elements, then the inner iteration also visits each of the Z-min elements in the current level. For each such Z-min element, the depth value which is written into that element is the nearest depth value in any of the Z-min elements which are covered by such Z-min element in the next finer granularity level…" – col. 14, ll. 48-67, and col. 15, ll. 1-6; col. 17, ll. 24-40).

It is noted that said Z-pyramid is considered to read on hierarchical Z value range (e.g., hierarchical Z buffer). It is noted that a single depth element 512 (e.g., pixel) is considered to read on a tile. It is noted that a respective Z-min and Z-max values for a given depth element are considered to read on a tile Z value range.

It would have been obvious to one skilled in the art, at the time of the Applicant's invention, to incorporate the teachings of Greene et al. into the method taught by Aila et al., because such incorporation, as taught by Greene et al., would allow for the quicker rejection of hidden geometry ("...hierarchical data structures make it possible to reject hidden geometry very rapidly while rendering visible geometry with the speed of scan conversion..." – Abstract) and would not prove difficult to implement ("...The technique is not difficult to implement..." – col. 4, ll. 2-4) resulting in a more efficient system. Furthermore, Aila et al. teach the use of a rasterizer (e.g., rasterizer 514) for converting a polygon into pixels or samples inside the polygon (p. 5, ¶ 69). Greene et al. teach a means of accelerating scan conversion ("...The method uses ... in order to accelerate scan conversion..." – Abstract). It is noted that scan conversion is considered an element of rasterization and thus through such incorporation it would provide a means of processing a greater amount of information in less amount of time resulting in improved efficiency.

In light of said incorporation it is implicitly taught that during the processing of a respective tile or group of tiles that respective information (e.g., depth information, shadow/stencil information, etc.) associated within said tile(s) is accessed. It is noted that the respective claim language fails to disclose what exactly constitutes "updating" and thus said accessing is considered to read on the limitation "updating the hierarchical Z value range and the stencil code in response thereto."

In light of said incorporation Aila et al. and Greene et al. teach determining whether to render a plurality of pixels within the tile based on the comparison of the tile

Z value range with the hierarchical Z value range and the (e.g., shadow information) stencil code (Aila et al. – p. 4, ¶s 53, 56, 58; Figs. 4, 5; Greene et al. – col. 3, ll. 61-64; col. 6, ll. 19-36; "In step 726, the new contents of the display buffer (FIG. 3) are displayed on the display (FIG. 2) and the render frame procedure 612 returns in a step 728 to the render sequential frames routine 602 (FIG. 6)…" – col. 14, ll. 44; Fig. 7). As illustrated in Fig. 7 step 726 (Display New Display Buffer) is dependent upon the processing performed in step 719 (Build Depth Buffer). It is noted that the respective claim language discloses "determining whether to render a plurality of pixels" but fails to disclose to what said pixels are rendered (e.g., rendered to a frame buffer, rendered to a frame buffer and then displayed on a display device, etc.).

7. In regard to claim 2 Aila et al. teach determining if a stencil test passes on at least one pixel (p. 7, ¶ 86) and Greene et al. teach determining if a hierarchical Z value test passes on at least one pixel (e.g., geometry is determined to be visible and is rendered; Abstract). The motivation disclosed in the rejection of claim 1 is incorporated herein.

8. In regard to claim 3 the rationale disclosed in the rejection of claim 2 is incorporated herein.

9. In regard to claim 4 Aila et al. teach killing the tile (e.g., skipping rasterization for a tile) when the stencil test fails (p. 7, ¶ 86). It is noted that the respective claim language fails to disclose what exactly constitutes "killing the tile" and thus skipping rasterization for a tile is considered to read on killing said tile.

10. In regard to claim 5 Aila et al. teach wherein said tile Z value range contains a tile (e.g., z_{min}) MinZ and a tile (e.g., z_{max}) MaxZ (the rationale disclosed in the rejection of claim 1 is incorporated herein, specifically: p. 4, ¶ 53). Greene et al. teach wherein said tile Z value range contains a tile (e.g., Z-min) MinZ and a tile (e.g., Z-max) MaxZ and wherein said Z value range contains (e.g., any of the Z-min elements which are covered by such Z-min element in the next finer granularity level) a hierarchical cache MinZ and a (e.g., any of the Z-max elements which are covered by such Z-max element in the next finer granularity level) hierarchical cache MaxZ (the rationale disclosed in the rejection of claim 1 is incorporated herein, specifically: col. 6, ll. 9-36; col. 11, ll. 4-12; col. 14, ll. 48-67; col. 15, ll. 1-6; col. 17, ll. 24-40). The motivation disclosed in the rejection of claim 1 is incorporated herein. As disclosed in the rejection of claim 1 it is noted that a single depth element 512 (e.g., pixel) is considered to read on a tile and that a respective Z-min and Z-max values for a given depth element are considered to read on a tile Z value range.

11. In regard to claim 6 it is noted that the respective claim language fails to disclose what exactly constitutes a "background value" or a "stencil value." Aila et al. teach the use of a multiple-bit indicator for said stencil code ("...the shadow volume rasterization uses only a small subset of the 8-bit stencil buffer values ... a four bit stencil value is used..." – pp. 8, 9, ¶s 101, 102), which specifies a relation of a plurality of stencil values in the tile relative to a background value ("...the contribution of the light source is accumulated into the frame buffer by rendering the shadow mask from the stencil buffer..." – p. 7, ¶ 92; "In connection with Fig. 6 entries for storing stencil values (or,

more generally, shadow information) were discussed … tile-specific entries of a stencil buffer (or other information store) may be implemented as a combination of a Boolean value and a stencil value…" – p. 8, ¶ 99). It is noted that a "background value" is considered to read on shadow information which affects how a give pixel or pixels are rendered visually. It is further noted that that the respective claim language comprises open-ended language (e.g., comprising) and therefore the language "wherein the stencil code is a three bit data value" is not considered to read on "wherein the stencil code is only a three bit data value." It is further noted that a four bit data value is considered to include a three bit data value and therefore the respective claim limitations are considered to be met.

12. In regard to claim 7 the rationale disclosed in the rejection of claim 1 is incorporated herein. Aila et al. teach per-pixel processing (p. 5, ¶ 70). It is noted that each of said depth elements 512 are considered to represent respective pixel elements 204 (Greene et al. – Figs. 2, 5A) and therefor the respective teachings of Greene et al. are considered to result, at least in part, in per-pixel processing.

13. In regard to claim 8 the rationale disclosed in the rejections of claims 1 and 6 are incorporated herein.

14. In regard to claim 9 Aila et al. teach generating an indicator (e.g., Boolean boundary value) to indicate whether to render the plurality of pixels within the tile ("If the Boolean boundary value in the temporary tile classification buffer is TRUE for a tile, this needs to be rasterized using a finer resolution, for example, using per-pixel resolution.

Otherwise the rasterization can be skipped, because the entire tile is either in shadow or lit..." – p. 7, ¶ 86).

15. In regard to claim 10 the rationale disclosed in the rejection of claim 7 is incorporated herein.

16. In regard to claim 11 Aila et al. teach comparing the stencil code (e.g., shadow information) to a stencil value (the rationale disclosed in the rejection of claim 6 is incorporated herein) and a stencil mask (e.g., shadow information; "...Often information about shadows is called a shadow mask..." – p. 1, ¶ 8; "...There are two alternatives for determining shadows masks, a Z-pass and a Z-fail method..." – p. 1, ¶ 12; "A shadow mask is typically stored in a stencil buffer, and the following description is consistent with this practice..." – p. 3, ¶ 53; "...The minimum and maximum stencil values are also useful for generic computations using stencil buffer..." – p. 8, ¶ 101). It is noted that the respective claim language fails to disclose what exactly constitutes a "stencil code" and a "stencil mask." Thus, a stencil code and stencil mask are considered to read on shadow information.

17. In regard to claim 13 the rationale disclosed in the rejection of claim 5 is incorporated herein.

18. In regard to claim 19 the rationale disclosed in the rejection of claim 7 is incorporated herein.

19. In regard to claim 23 the rationale disclosed in the rejection of claims 1, 5 and 11 are incorporated herein. It is implicitly taught hat said tiles have a respective location in space during processing. It is noted that a comparator (Aila et al. – Fig. 5, element 501)

is considered coupled to a hierarchical Z buffer (Aila et al. – Fig. 5, element 521; Greene et al. – Fig. 1, element 104), stencil cache (Aila et al. – Fig. 5, element 523) and hierarchical Z buffer and stencil cache updater (Aila et al. – Fig. 5, element 510).

20. In regard to claim 24 the respective claim language fails to disclose what exactly constitutes a "relative" relationship between the visibility of a plurality of pixels and a stencil mask and a hierarchical Z plane. Thus, it is noted that visible pixels on a given hierarchical Z plane which undergo shadow processing is considered to read on a relative relationship. The rationale disclosed in the rejection of claim 9 is incorporated herein.

21. In regard to claim 26 the rationale disclosed in the rejections of claim 1 and 11 are incorporated herein.

22. In regard to claim 27 the rationale disclosed in the rejections of claims 8, 11 and 13 are incorporated herein.

23. In regard to claim 30 the rationale and motivation disclosed in the rejection of claim 27 is incorporated herein. Aila et al. fails to explicitly teach generating a signal indicating that a detailed depth test is not required because all pixels of the tile are known to be visible in the hierarchical Z plane. It is noted that the respective claim language fails to disclose what exactly constitutes a "detailed depth test" and therefore a "detailed depth test" is considered to read on a "depth test." Greene et al. teach indicating that a depth test is not required because all pixels of the tile are known to be visible in the hierarchical Z plane (col. 6, ll. 60-66; col. 7, ll. 1-4). The motivation disclosed in the rejection of claim 8 is incorporated herein.

Response to Arguments

24. In response to Applicant's remarks that the Office Action appears to allege that Greene et al. teach both a hierarchical Z value range and a tile Z value range it is noted that the Examiner agrees. However, it is noted that Greene et al. is primarily relied upon to address the limitations directed to a hierarchical Z value range. The Applicant is directed to the respective above rejections which have further been clarified to address the Applicant's remarks.

25. In response to Applicant's remarks that the Office Action alleges that the Z-max and Z-min values of any particular depth element 512 in the Z-pyramid are equivalent to the claimed tile Z range and that the Z-max and Z-min values in the next finer granularity level of the same Z-pyramid somehow represent a hierarchical Z value range it is noted that the Examiner, for the most part, agrees. In response to Applicant's remarks that this position constitutes clear error for at least two reasons: (1) it is inconsistent and (2) the Z values in the next finer granularity levels are not compared with any alleged tile Z values as required by the claims it is noted the Examiner does not agree.

In response to points (1), (2) and Applicant's remarks that it is inconsistent to suggest that some such depth elements are tile Z value ranges while other depth elements are hierarchical Z value ranges it is the position of the Examiner that this is not at all inconsistent as not all Z value ranges taught by Greene et al. are processed the same at any given time. It appears to the Examiner that the Applicant is implying that all Z-min and Z-max value ranges taught by Green et al. are given equal consideration

at all times. This is simply not the case and is clearly evidenced by the teachings of Greene et al., specifically: "...Within each level, an inner iteration is performed to visit each of the depth elements (Z-max elements) in that level. For each such Z-max element, the depth value which is written into that element is the farthest depth value in any of the Z-max elements which are covered by such Z-max element in the next finer granularity level. If the depth buffer 502 also includes Z-min elements, then the inner iteration also visits each of the Z-min elements in the current level. For each such Z-min element, the depth value which is written into that element is the nearest depth value in any of the Z-min elements which are covered by such Z-min element in the next finer granularity level..." (col. 14, ll. 48-67, and col. 15, ll. 1-6; col. 17, ll. 24-40). In other word there is a clear distinction made between the depth values of a given element within a respective level and the depth values which belong to all other levels which are different from the level currently being processed.

26. In response to Applicant's remarks that Aila et al. fails to cure the deficiencies of Greene et al. it is noted that Aila et al. was not and currently is not introduced to addressed the deficiencies of Greene et al.

27. Applicant's remarks have been fully considered but they are not deemed persuasive.

28. The Applicant is encouraged to schedule an interview with the Examiner to discuss the application if the Applicant feels it would be beneficial.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PETER-ANTHONY PAPPAS whose telephone number is 571-272-7646. The examiner can normally be reached on M-F 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Peter-Anthony Pappas/
Primary Examiner, Art Unit 2628